

Fig. 1

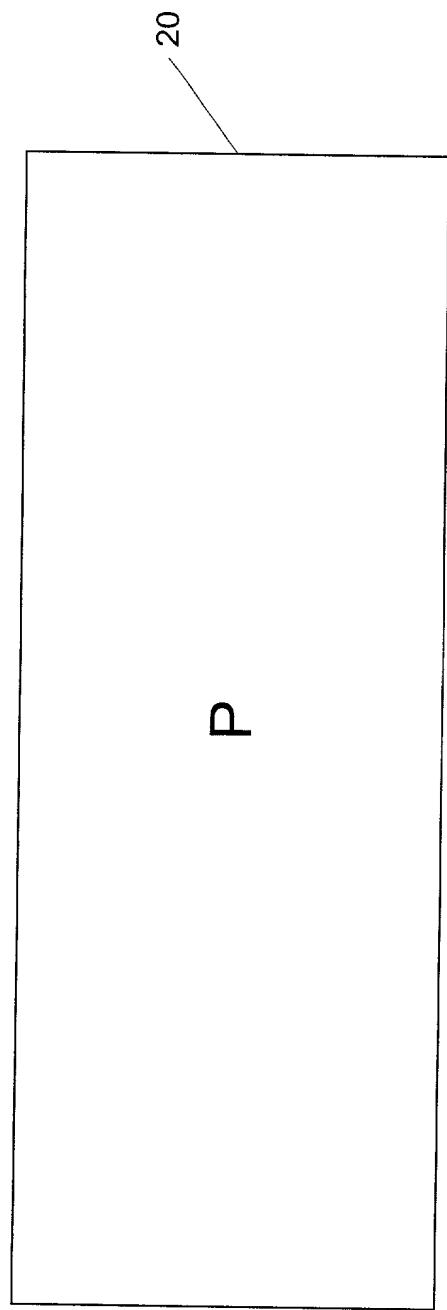
[illegible]

Fig. 2a

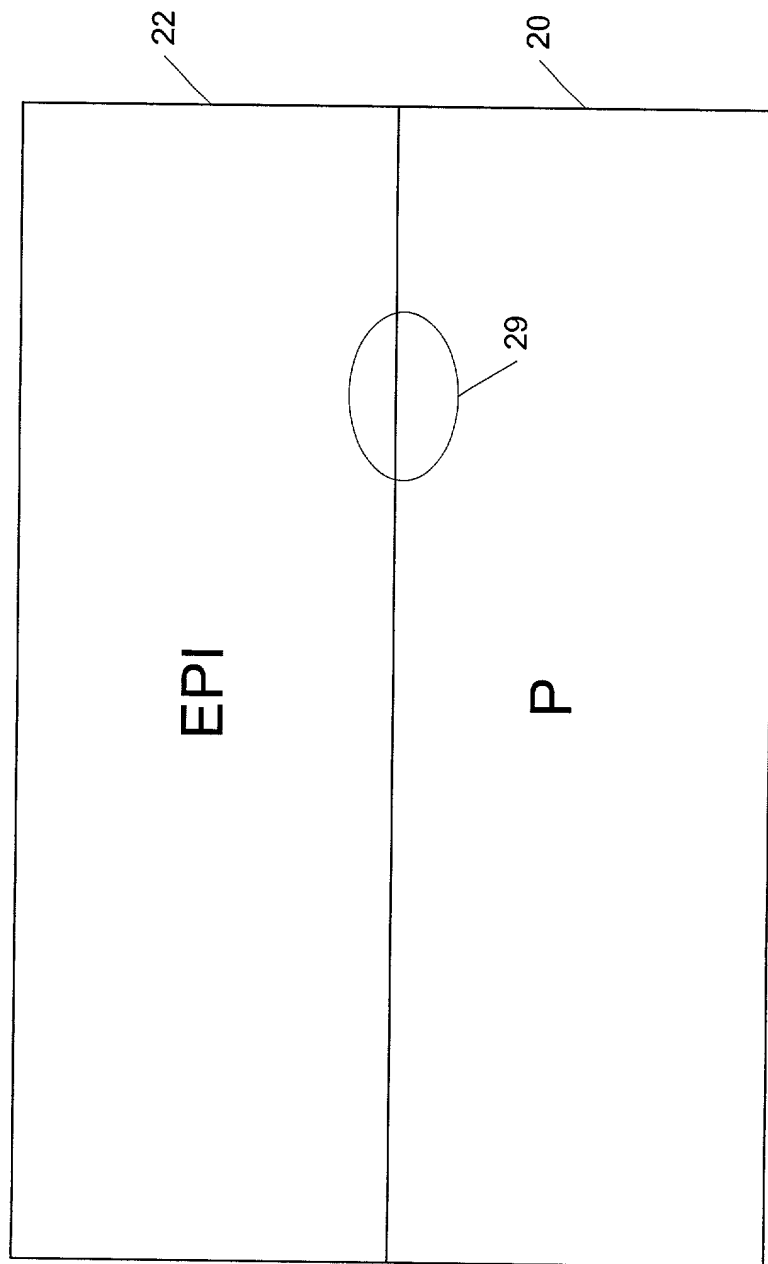


Fig. 2b

Fig. 2c

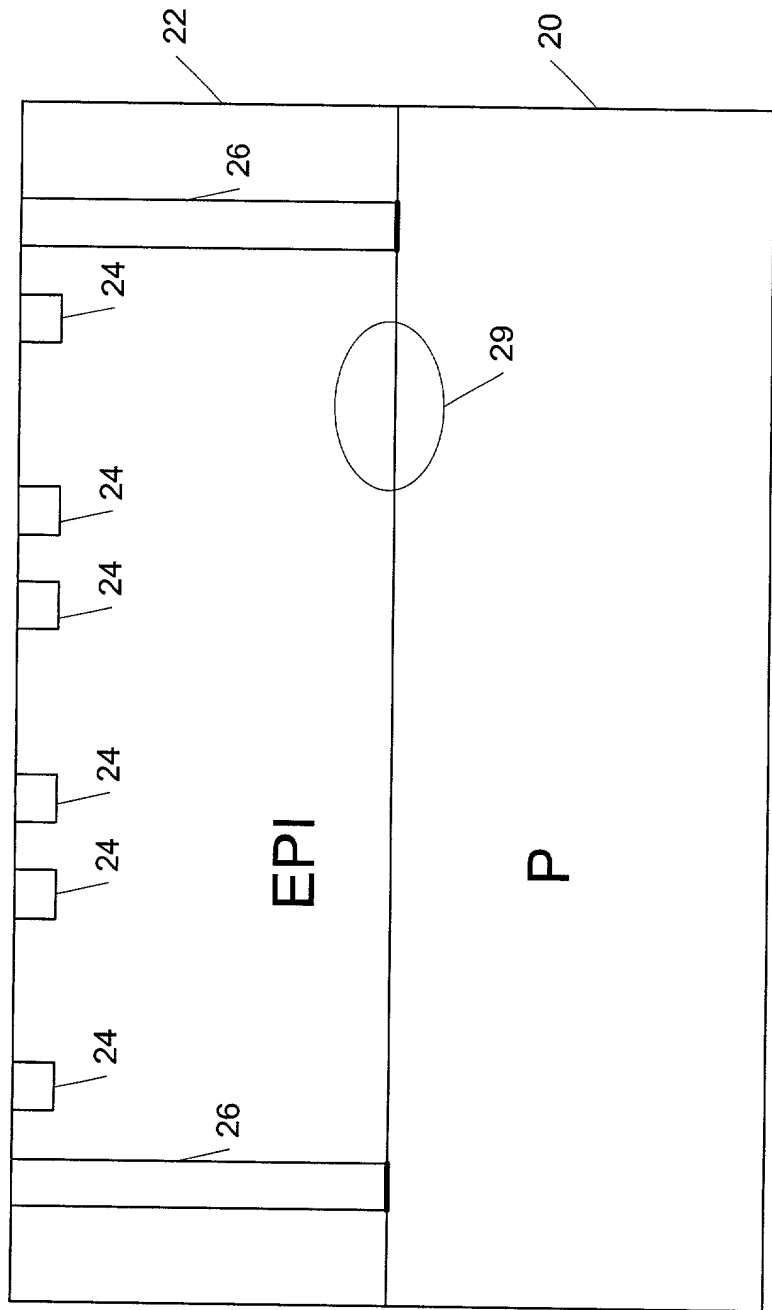


Fig. 2d

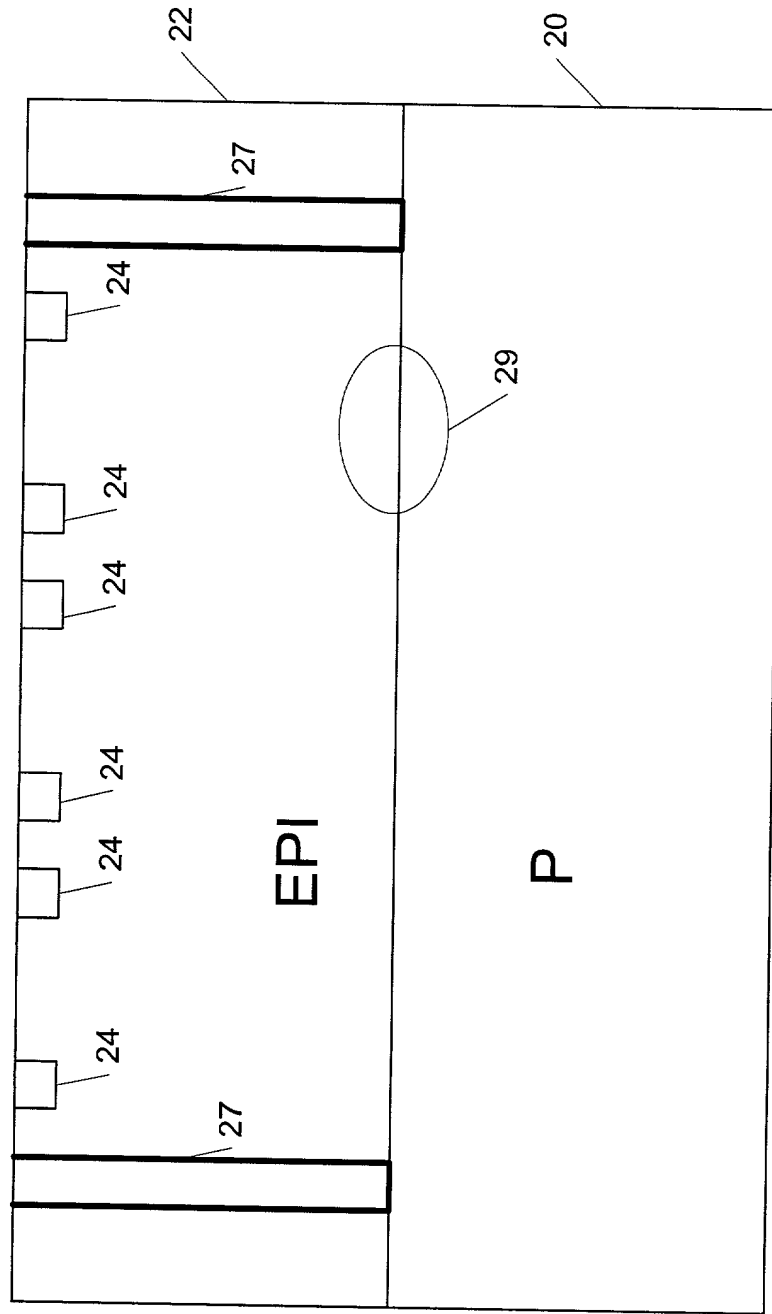


Fig. 2e

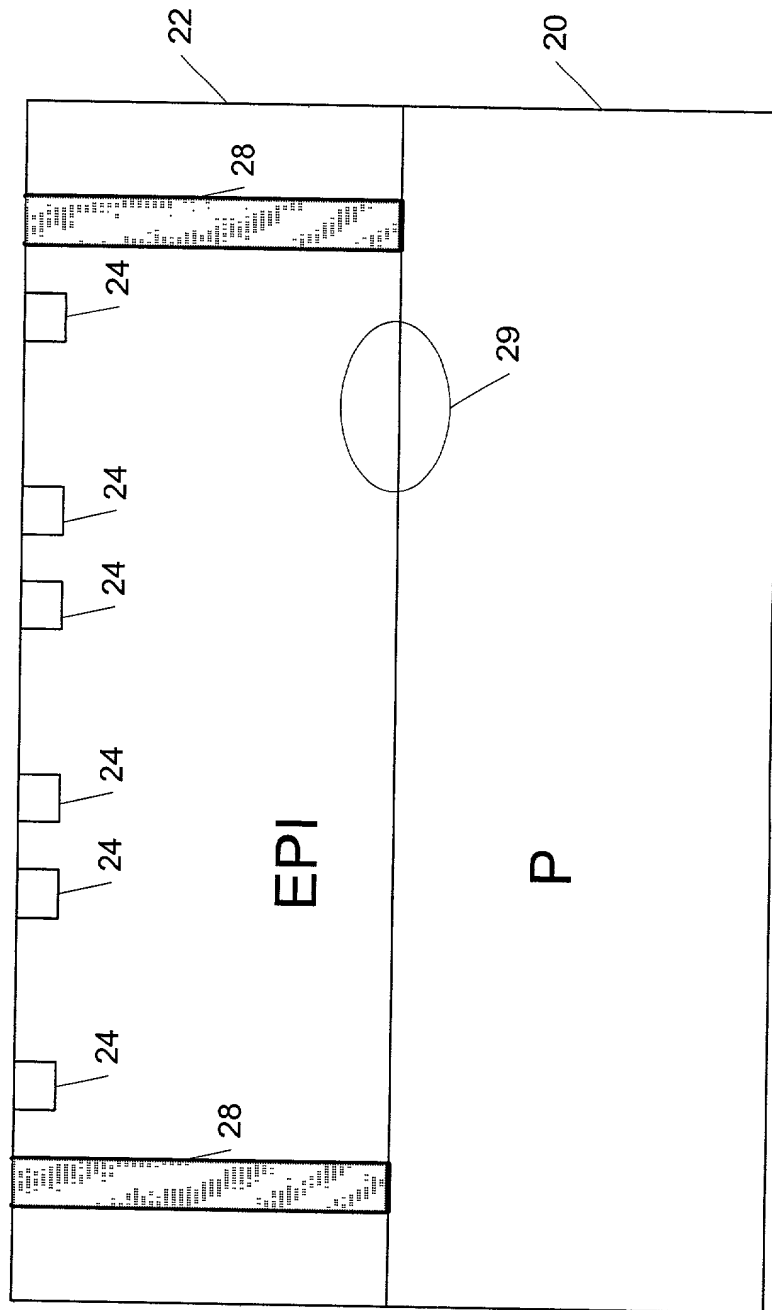


Fig. 2f

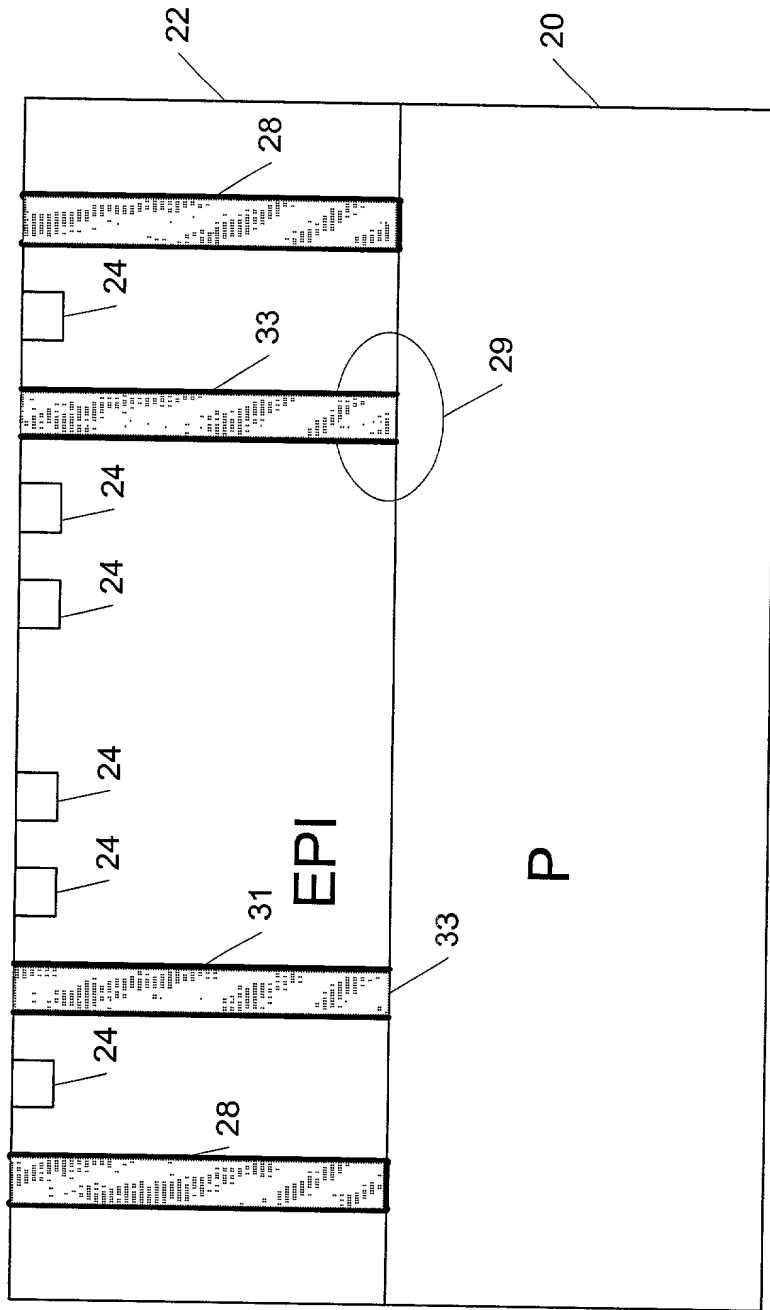


Fig. 2g

⊗ L LENGTH
INTO
PAPER

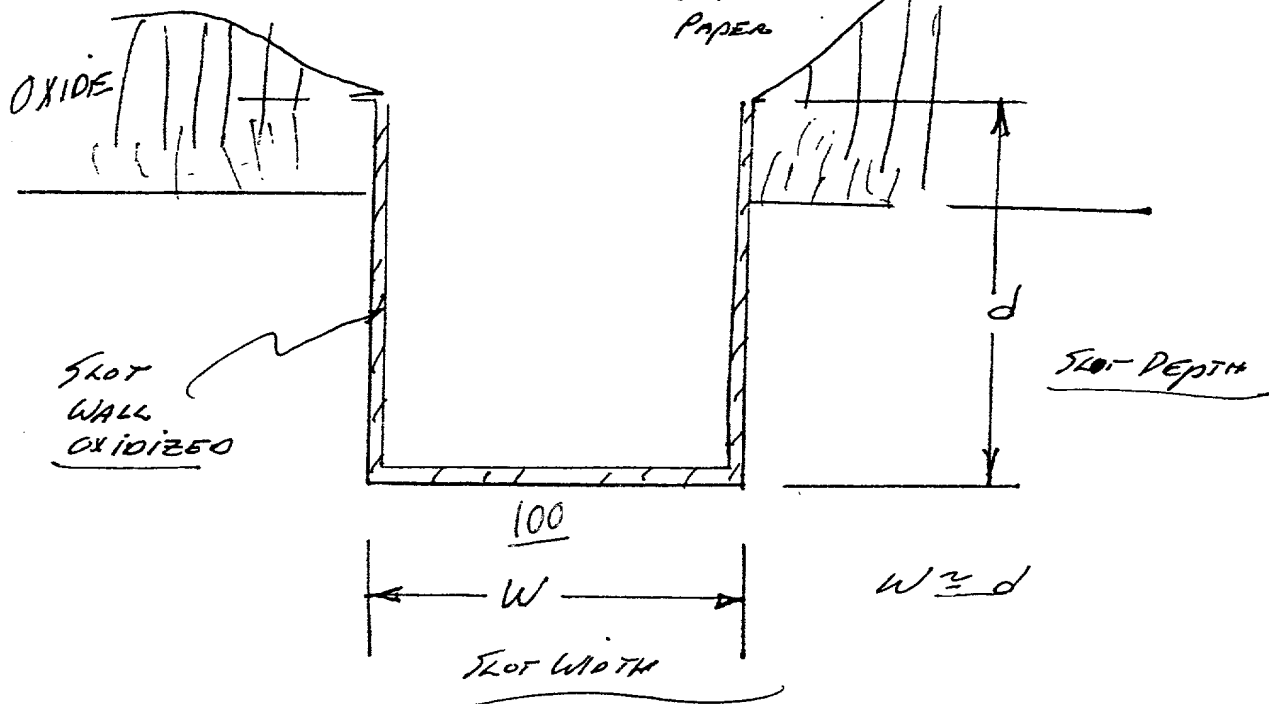


Fig. 3

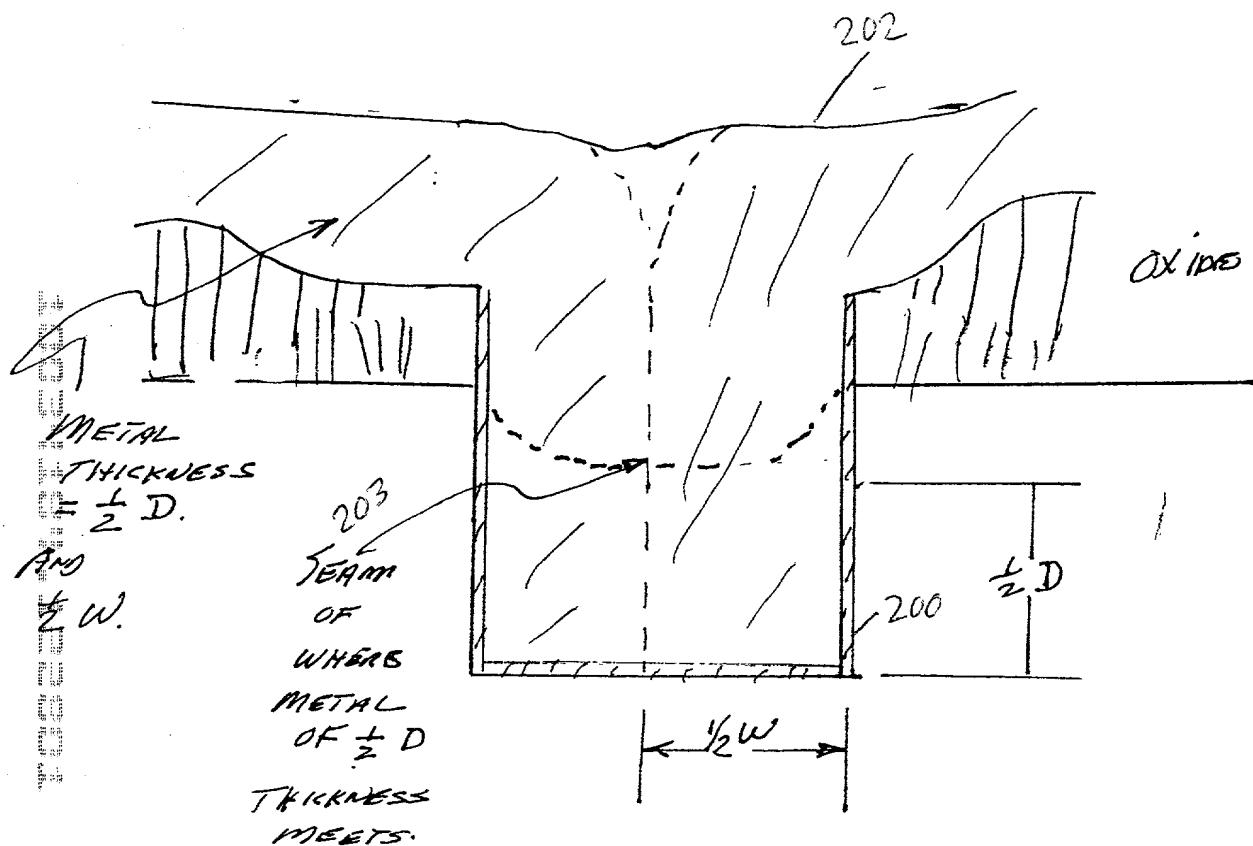
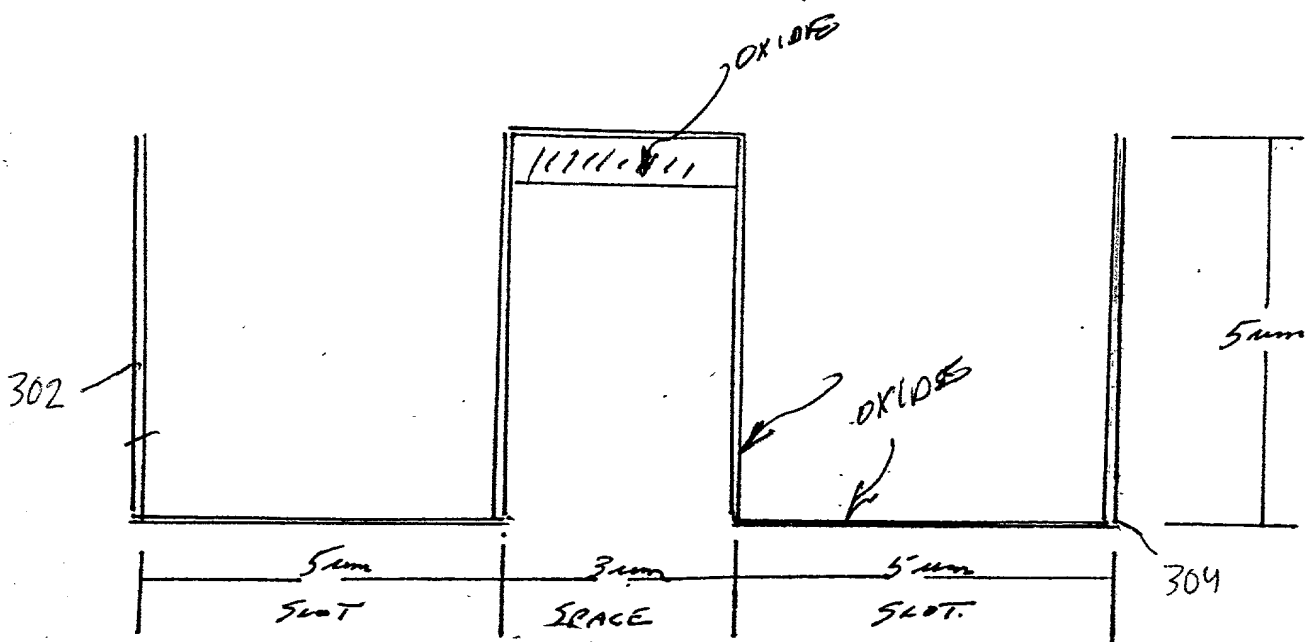
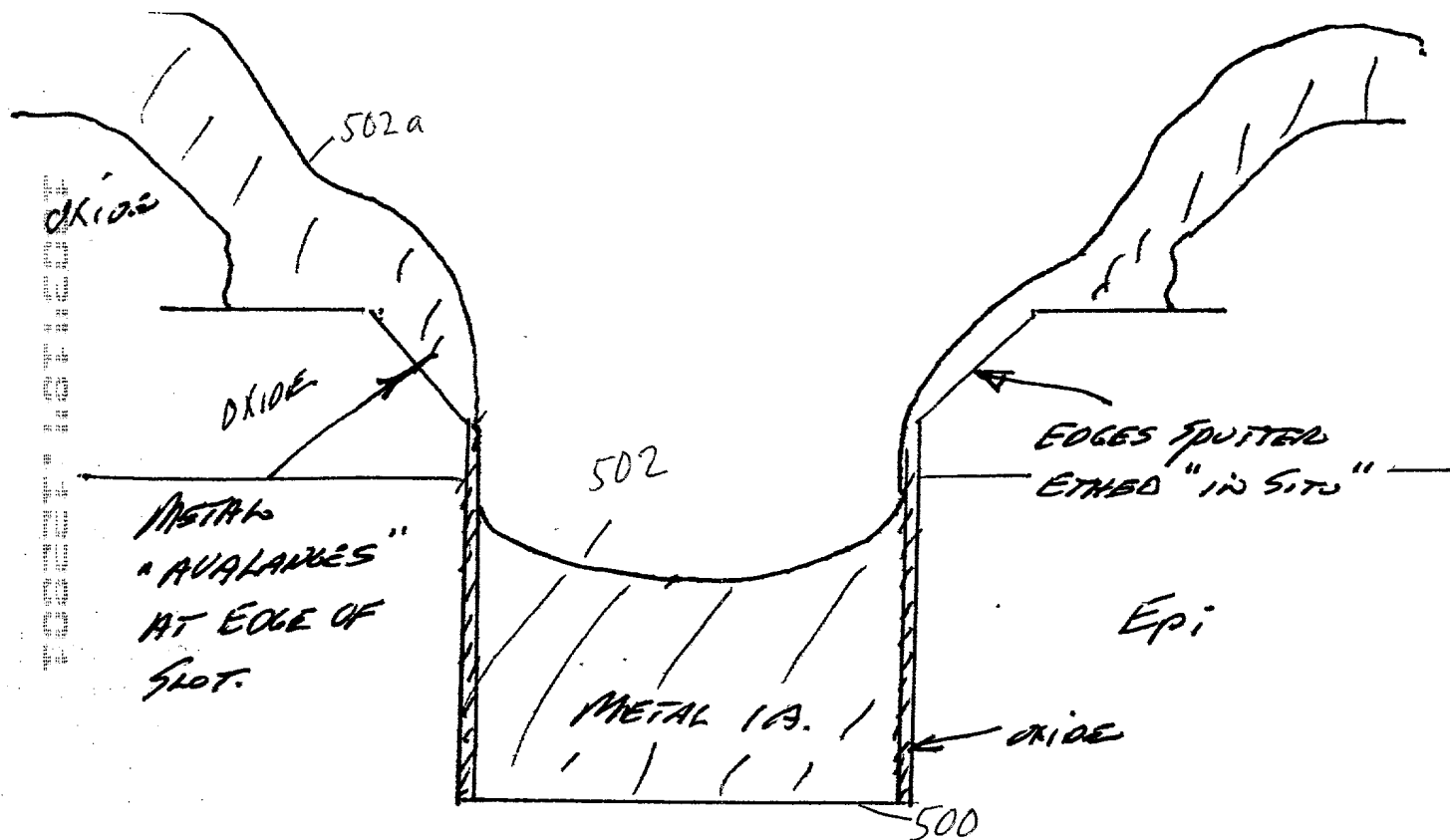


Fig. 4



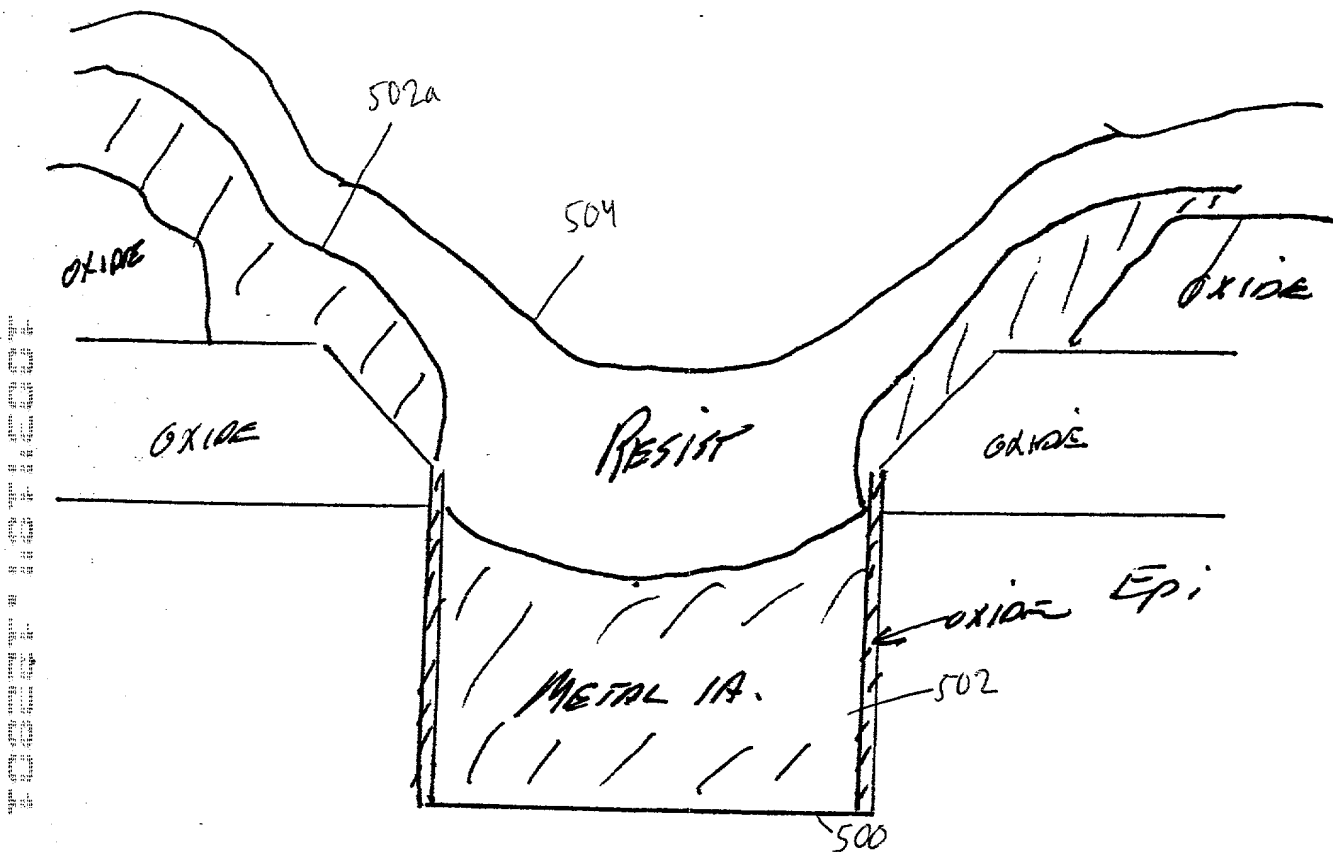
DOUBLE SLOT FOR
DOUBLE WIDTH OF METAL.
3mm SPACE BETWEEN SLOTS

Fig. 4a



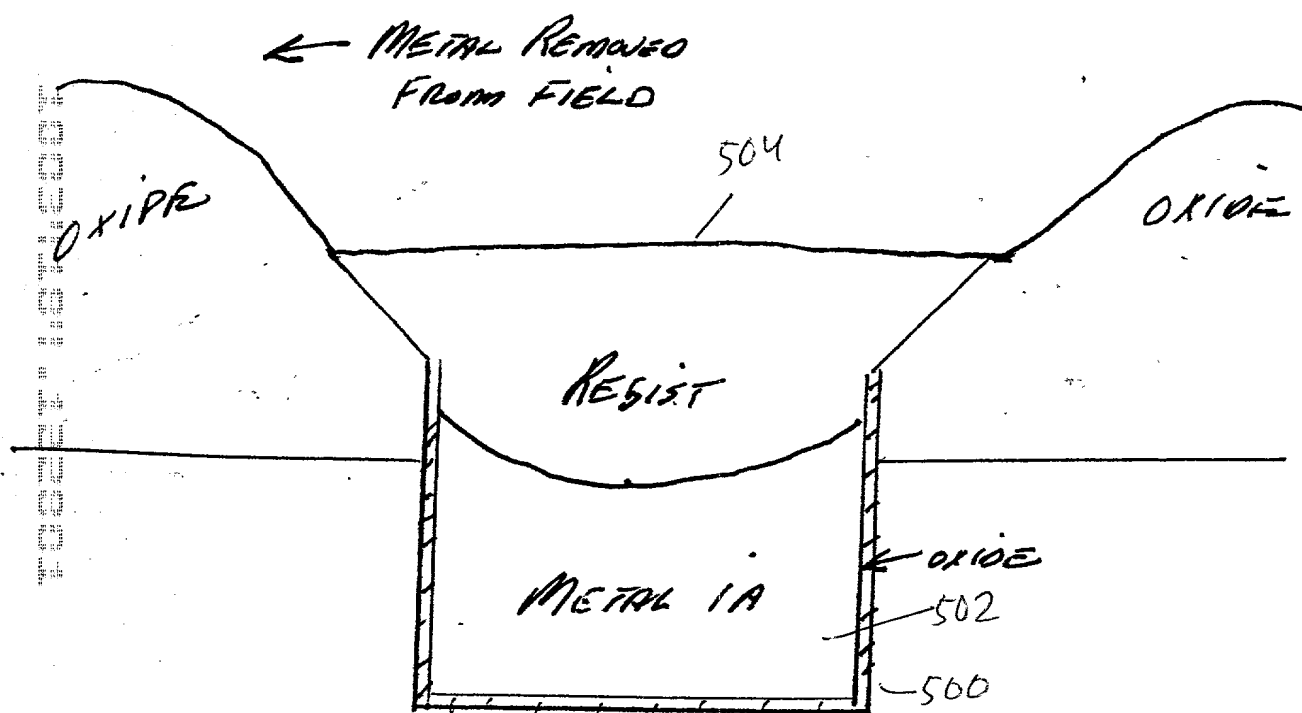
Prior TO METAL 1A BEING
 SPUTTERED, THE EDGES OF THE OXIDES
 ARE SPUTTERED ETCHED "IN SITU" &
 1A DEPOSITED

Fig. 5



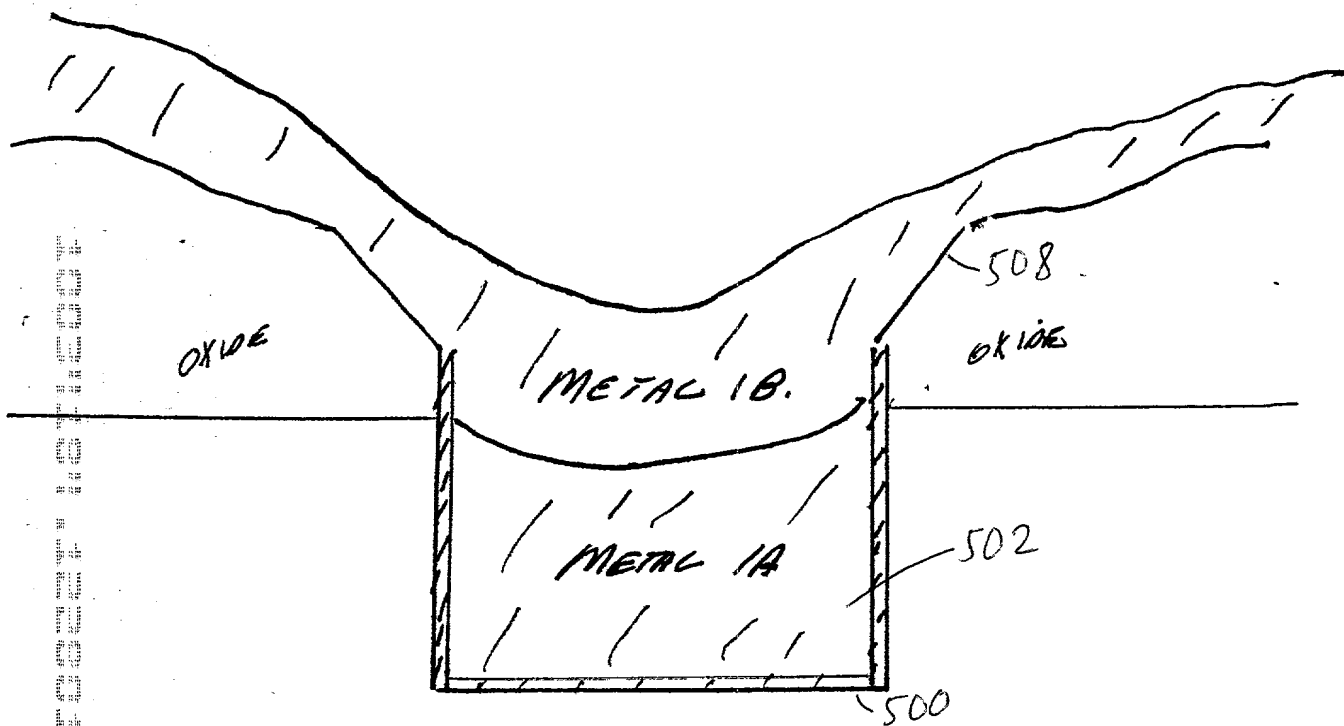
RESIST COATING - THICK IN THE
SLOTS

Fig. 6



RESIST PATTERN ETCHED.
 LEAVING RESIST IN SLOTS.
 FIELD METAL ETCHED OFF.

Fig. 7



RESIST STRIPPED & SECOND
METAL 1B SPUTTER DEPOSITED

Fig. 8

FIG. 9 is a cross-sectional view of a semiconductor device. The device includes a substrate 500, a first metal layer 502, a second metal layer 508, and a third metal layer 512. A dielectric layer 510 is formed over the first metal layer 502, and a deposited dielectric layer 513 is formed over the second metal layer 508. An oxide layer 514 is formed over the third metal layer 512. The first metal layer 502 is formed over the substrate 500, the second metal layer 508 is formed over the first metal layer 502, and the third metal layer 512 is formed over the second metal layer 508. The dielectric layer 510 is formed over the first metal layer 502, and the deposited dielectric layer 513 is formed over the second metal layer 508. The oxide layer 514 is formed over the third metal layer 512.

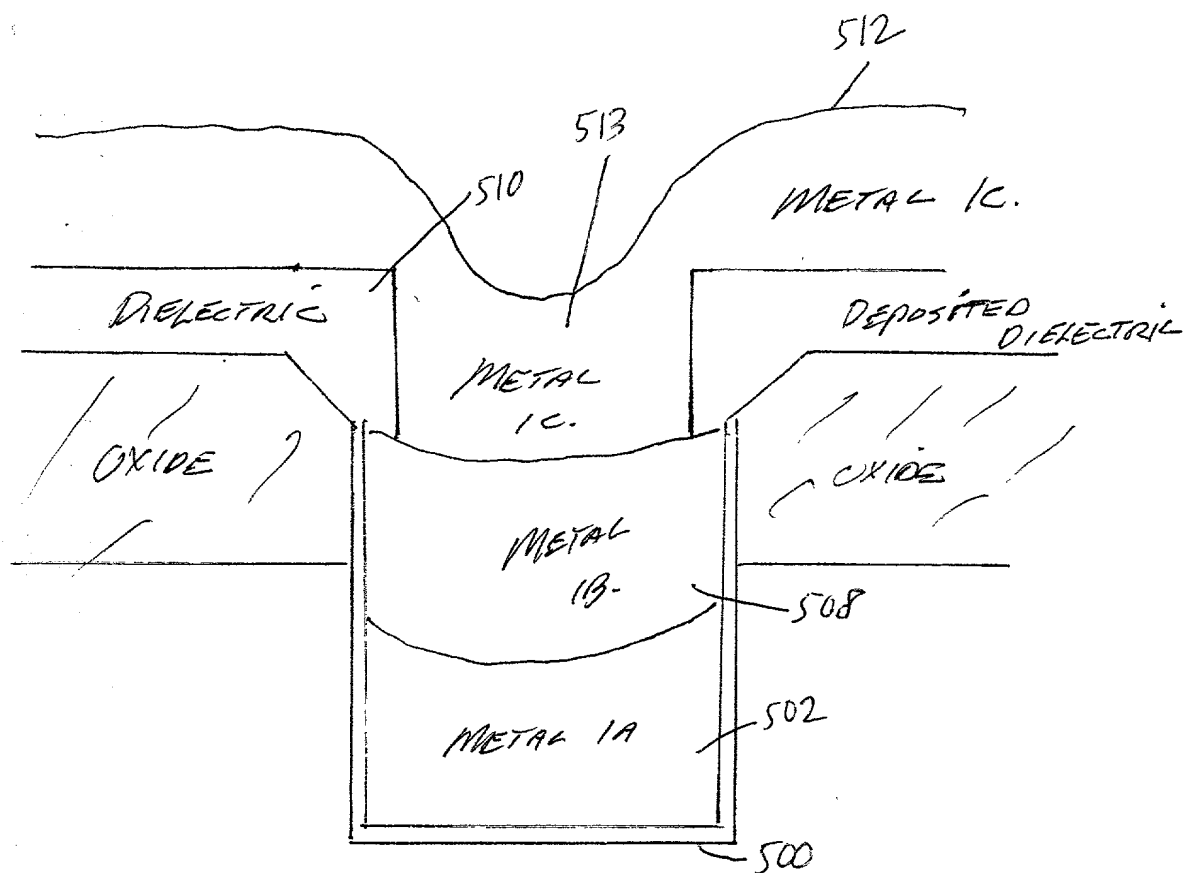


Fig. 9

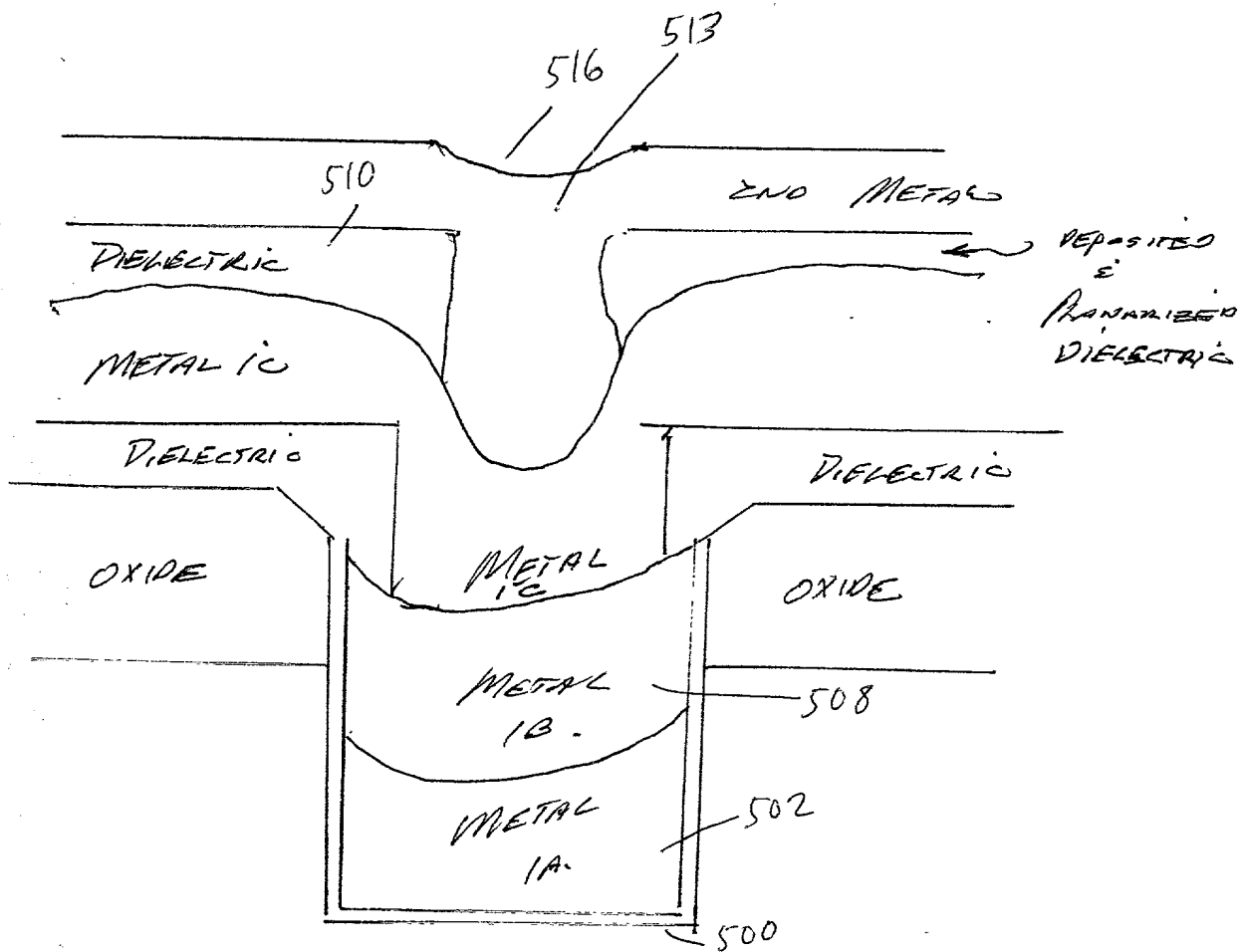
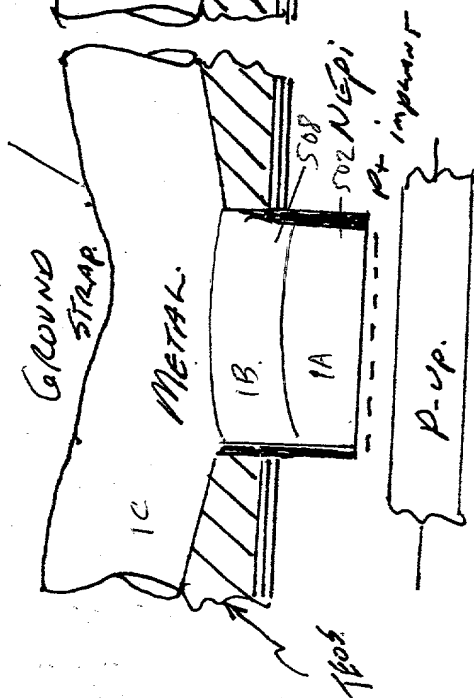


Fig. 10

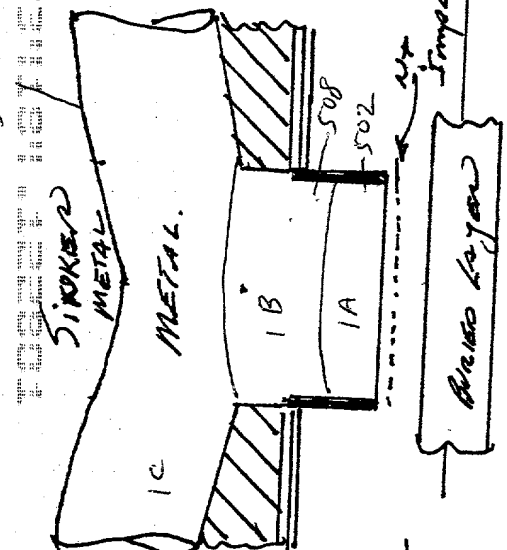
512



604

GROUND STRAP

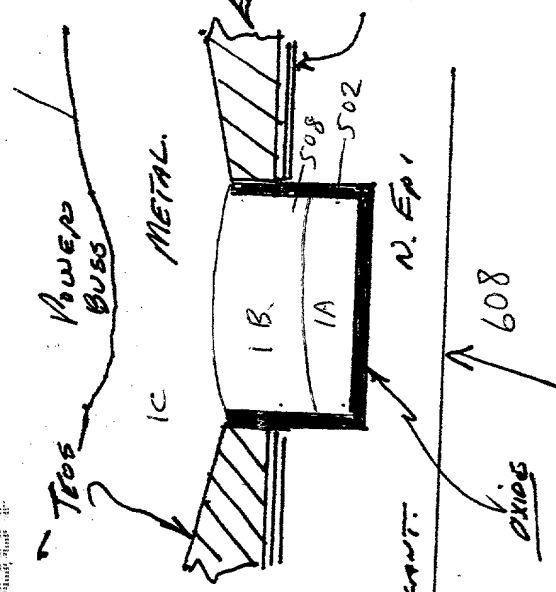
512



606

DRAIN/Buffer Layer / N+ IMPURANT

512



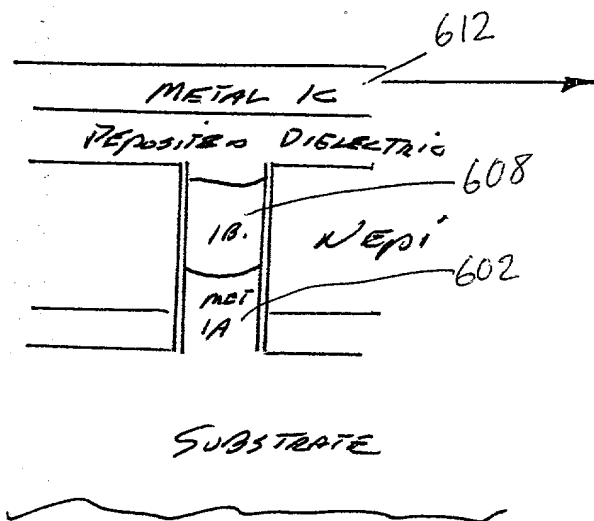
608

POWER BUSS

GROUND STRAP / Power Buss / DRAIN METAL SINKER

THIN LAYER OF DIELECTRIC
 FOLLOWED BY 9000 Å TEOS - POLISH -
 SLOTT MASK - METAL.
 METAL 15"-20 nm deposited

Fig. 11 POWER METAL.



METAL IC
 CONNECTS AN ISOLATED
 ISLAND TO ADJACENT
 ISOLATED EPI ISLANDS
 AND CROSSES OVER THE
 ISOLATION GROUND
 STRAP BY NOT OPENING
 A VIA IN THIS PORTION
 TO ALLOW IC TO BE
 ISOLATED FROM GROUND.

Fig. 12